UE From nanofabrication in research laboratories to VLSI

Niveau d'étude
Bac +5

ECTS
3 crédits

Composante
UFR PhITEM (physique, ingénierie, terre, environnement, mécanique)

Période de l'année
Toute l'année

- **Langue(s) d'enseignement:** Anglais
- **Ouvert aux étudiants en échange:** Oui
- **Code d'export Apogée:** PAX9NPAJ

Présentation

Description

Part I Nanofabrication in research labs:

Yannick Le Tiec (CEA) Franck Bassani (CEA) Philippe Rodriguez (CEA)

This part will cover the main nanofabrication and characterization techniques used in clean-rooms in research laboratory and semi-industrial environments for the fabrication of current and future semiconductor devices. The principles of these techniques will be presented and illustrated through concrete examples obtained in the clean-rooms of the Minatech Campus in Grenoble. This course will provide you with the basics of technological steps, thin film deposition techniques, lithography processes, and advanced characterization used during the fabrication of single devices up to their large-scale integration.
Content :

- Substrates/Materials (Si / Ge / SiGe / SOI / sSOI / Si28 / III-V….)
- Surface preparation (Batch / Single Wafer – Baths / Sprays / Cryogenics /…)
- Thin film deposition of semiconductors, insulators and metals (PVD / CVD / ECD /…
- Lithography (Photo / E-beam / Imprint) and etching (Wet / Dry) processes
- Ion implantation
- Chemical Mechanical polishing

- Molecular bonding (Wafer to Wafer / Hybrid bonding / Die to wafer / ….)
- Characterisation techniques (SPM / SEM-EDX / XRF / Ellipsometry / XPS / XRF / PL / Raman / XRD / …)

Part II : VLSI nanofabrication processes :

Maud Vinet (Quobly)

This second part describes the devices that are currently used and developed to sustain Moore's law: it spans the transistor technologies from bulk, to Finfet and FDSOI with their pros and cons and how they are manufactured, with a quick overview of the semiconductor industry players. It also describes the evolution of Moore's law and how it has moved from transistor to memory centric after having hit the limits of scaling, we have switched from dimensions scaling only to the introduction of new computing paradigms such as in memory computing to sustain the performance improvement of integrated circuits. Finally, it screens all the devices that are developed in order to overcome scaled transistors limitations with a strong emphasis on silicium spin qubits seen as a major contender to enable quantum computing.

Heures d'enseignement

UE From nanofabrication in research laboratories to VLSI - CM/TD	Cours magistral - Travaux dirigés	24h

Pré-requis recommandés

Semiconductor Physics

Période : Semestre 9

Infos pratiques

Lieu(x) ville

› Grenoble

Campus

› Grenoble - Domaine universitaire